In the Drawings:

Please replace Figs. 1 –21 with the enclosed Replacement sheets of formal drawings.

Fig. 1

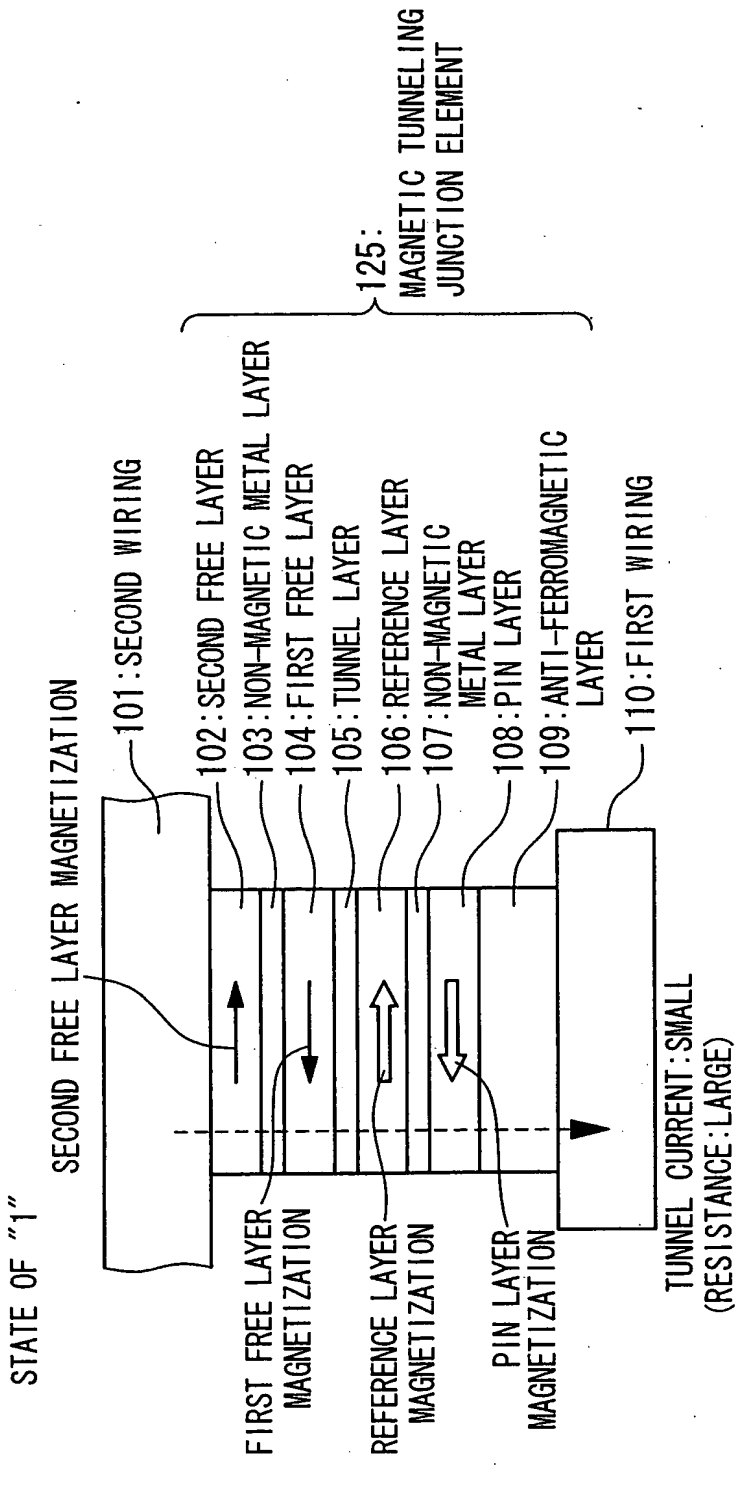

125: MAGNETIC TUNNELING JUNCTION ELEMENT
101:SECOND WIRING
102:SECOND FREE LAYER
103:NON-MAGNETIC METAL LAYER
104:FIRST FREE LAYER
105:TUNNEL LAYER
106:REFERENCE LAYER
107:NON-MAGNETIC METAL LAYER
108:PIN LAYER
109:ANTI-FERROMAGNETIC LAYER
110:FIRST WIRING
STATE OF "1"
SECOND FREE LAYER MAGNETIZATION
FIRST FREE LAYER MAGNETIZATION
REFERENCE LAYER MAGNETIZATION
PIN LAYER MAGNETIZATION
TUNNEL CURRENT:SMALL
(RESISTANCE:LARGE)

Fig. 2

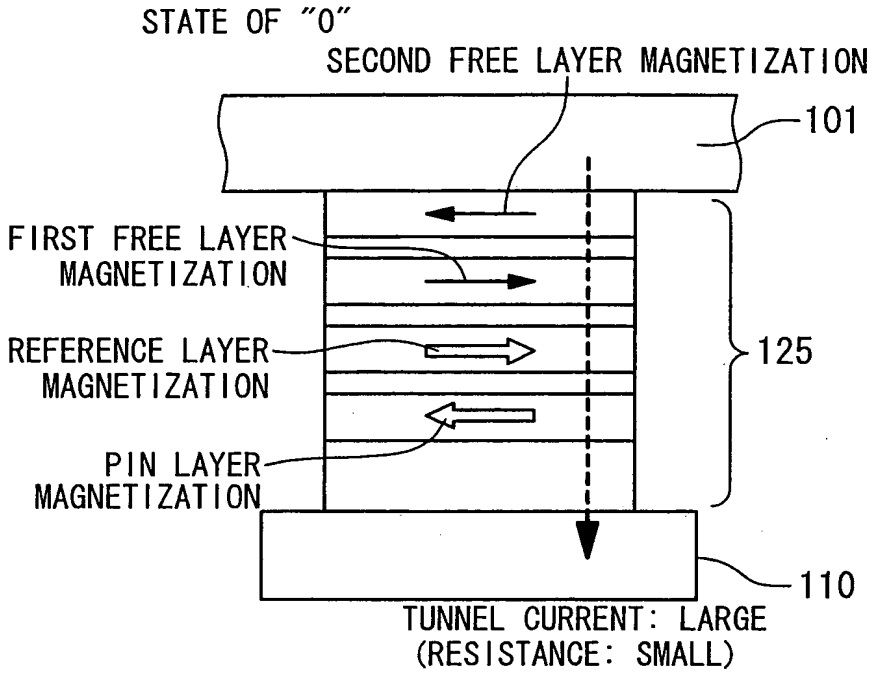

STATE OF "0"
SECOND FREE LAYER MAGNETIZATION
101
FIRST FREE LAYER MAGNETIZATION
REFERENCE LAYER MAGNETIZATION
PIN LAYER MAGNETIZATION
125
110
TUNNEL CURRENT: LARGE
(RESISTANCE: SMALL)

Fig. 3

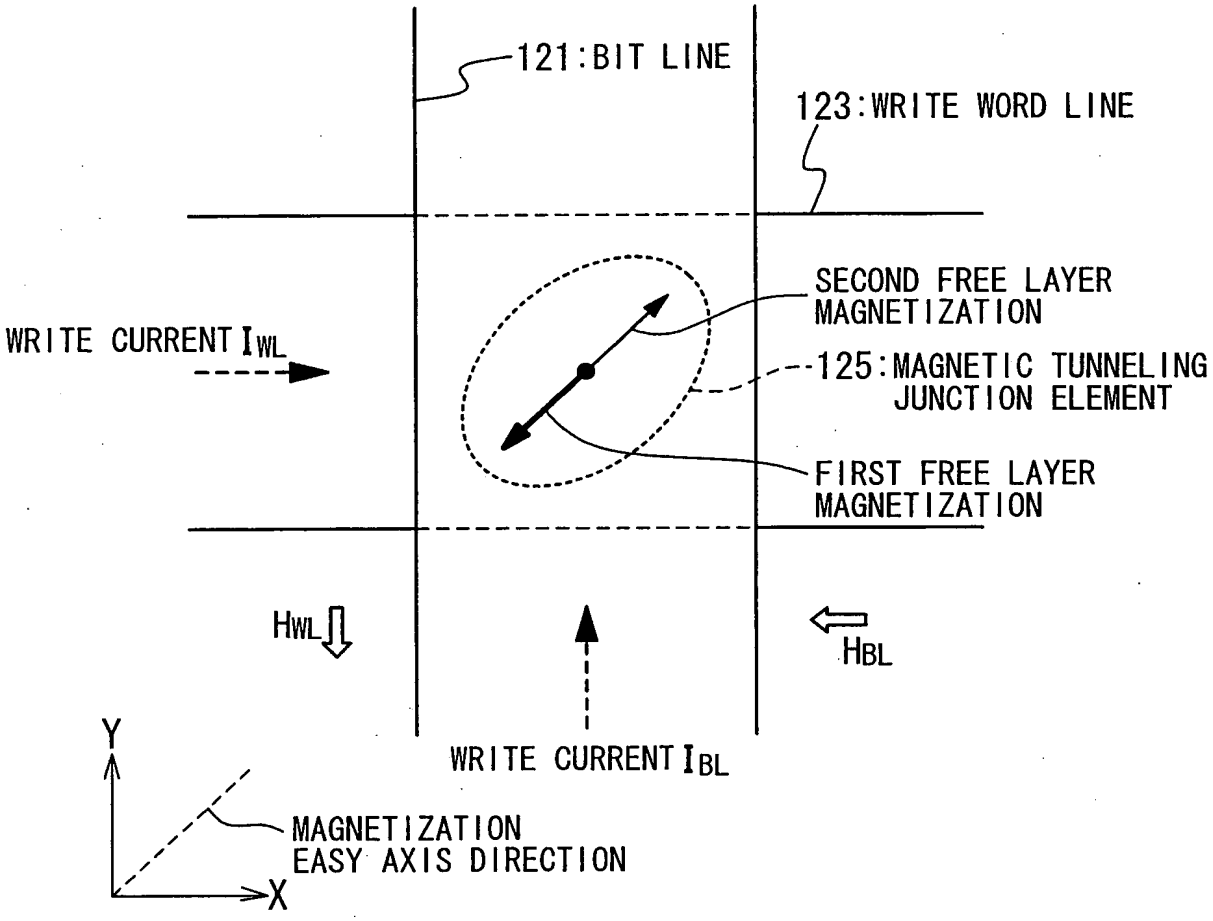

121:BIT LINE
123:WRITE WORD LINE
SECOND FREE LAYER MAGNETIZATION
125:MAGNETIC TUNNELING JUNCTION ELEMENT
FIRST FREE LAYER MAGNETIZATION
WRITE CURRENT I_{WL}
H_{WL}
H_{BL}
WRITE CURRENT I_{BL}
Y
X
MAGNETIZATION EASY AXIS DIRECTION

Fig. 4

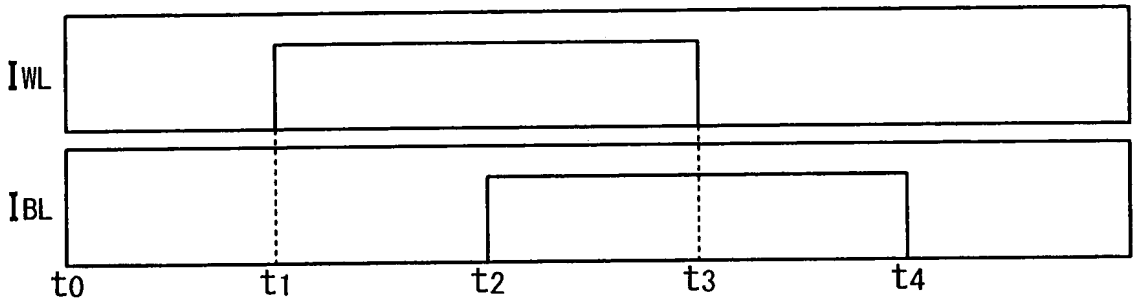


Fig. 5

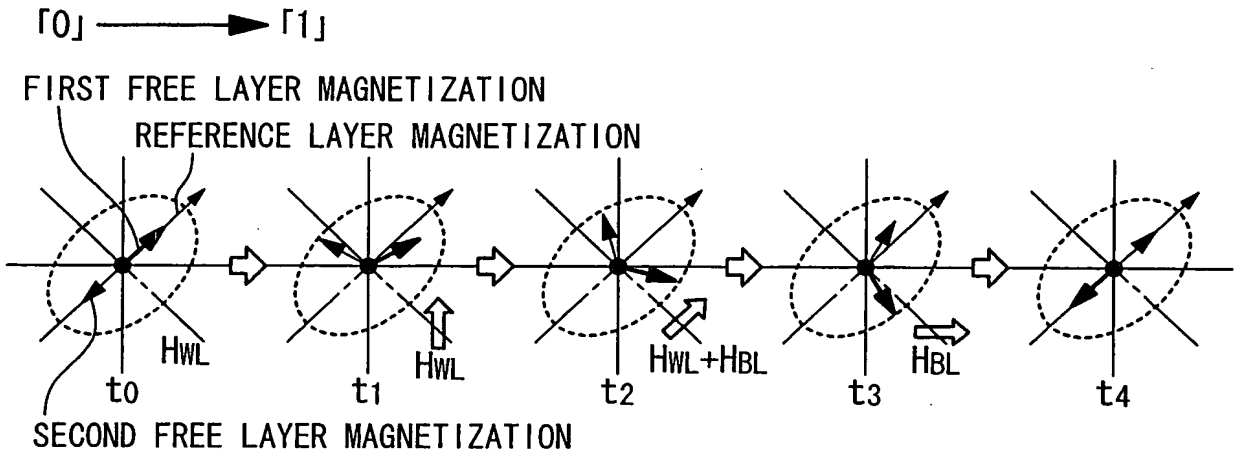

「0」 ——▶ 「1」
FIRST FREE LAYER MAGNETIZATION
REFERENCE LAYER MAGNETIZATION
HWL
HWL
HWL+HBL
HBL
t0
t1
t2
t3
t4
SECOND FREE LAYER MAGNETIZATION

Fig. 6

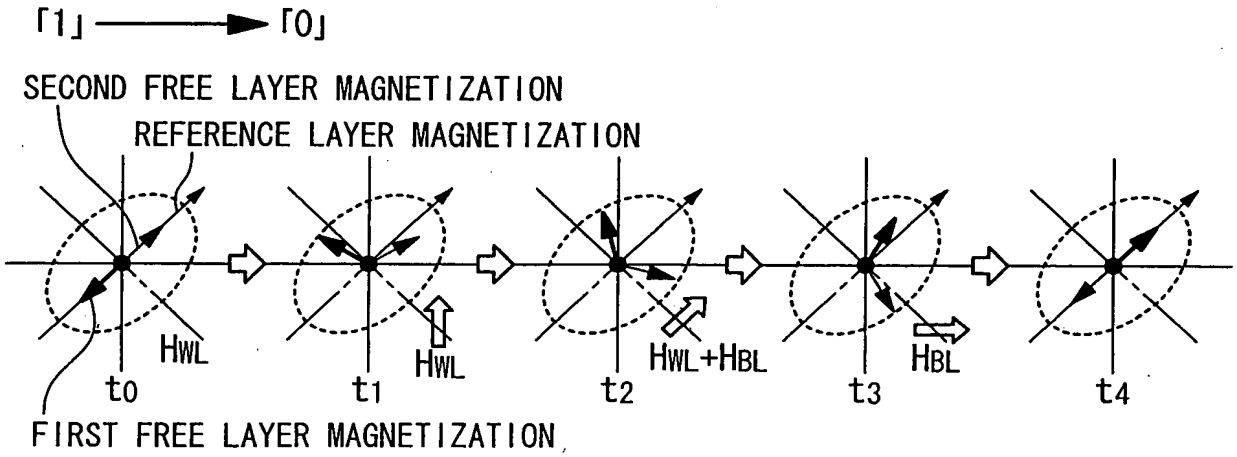

「1」 ——▶ 「0」
SECOND FREE LAYER MAGNETIZATION
REFERENCE LAYER MAGNETIZATION
HWL
HWL
HWL+HBL
HBL
t0
t1
t2
t3
t4
FIRST FREE LAYER MAGNETIZATION

Fig. 7

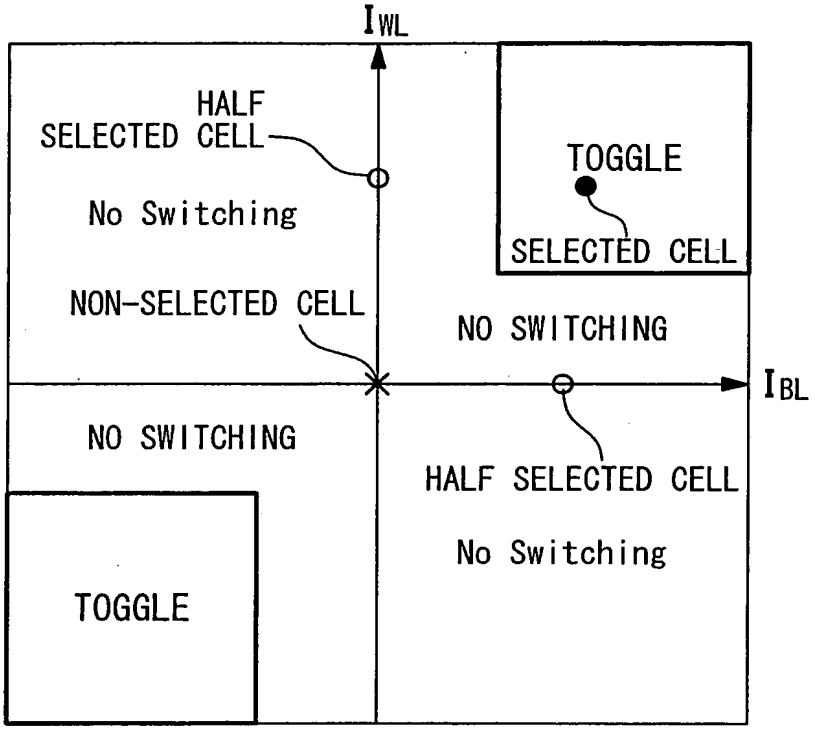

I_{WL}
HALF
SELECTED CELL
No Switching
NON-SELECTED CELL
TOGGLE
SELECTED CELL
NO SWITCHING
I_{BL}
NO SWITCHING
HALF SELECTED CELL
No Switching
TOGGLE

Fig. 8

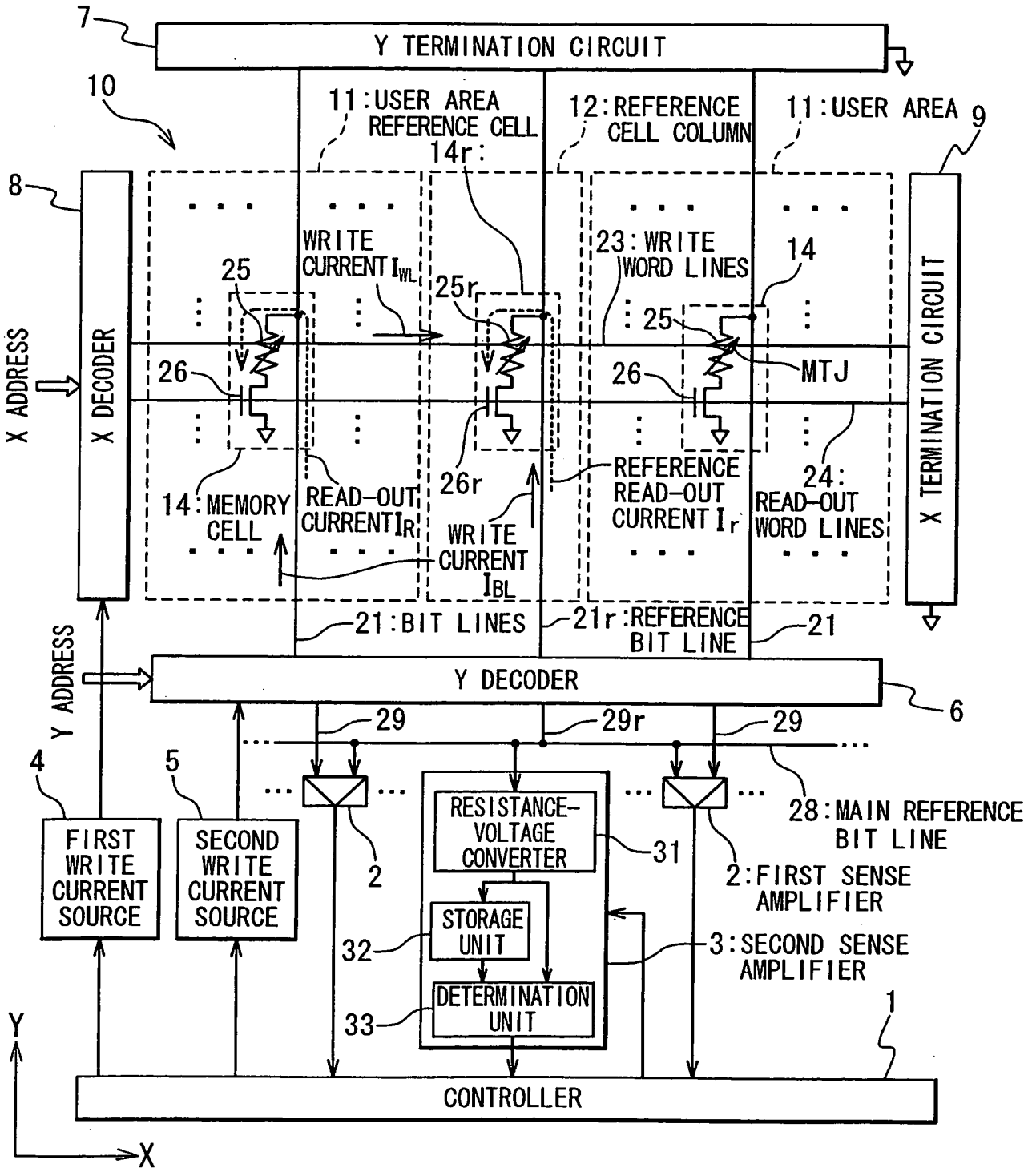

7
Y TERMINATION CIRCUIT
10
11:USER AREA
REFERENCE CELL
14r:
12:REFERENCE
CELL COLUMN
11:USER AREA
9
8
X ADDRESS
X DECODER
WRITE
CURRENT I_{WL}
25
25r
23:WRITE
WORD LINES
14
25
26
26
MTJ
X TERMINATION CIRCUIT
14:MEMORY
CELL
READ-OUT
CURRENT I_R
26r
WRITE
CURRENT
I_{BL}
REFERENCE
READ-OUT
CURRENT I_r
24:
READ-OUT
WORD LINES
21:BIT LINES
21r:REFERENCE
BIT LINE
21
Y ADDRESS
Y DECODER
6
29
29r
29
4
5
FIRST
WRITE
CURRENT
SOURCE
SECOND
WRITE
CURRENT
SOURCE
2
RESISTANCE-
VOLTAGE
CONVERTER
31
28:MAIN REFERENCE
BIT LINE
2:FIRST SENSE
AMPLIFIER
STORAGE
UNIT
32
3:SECOND SENSE
AMPLIFIER
DETERMINATION
UNIT
33
1
CONTROLLER
Y
X

Fig. 9

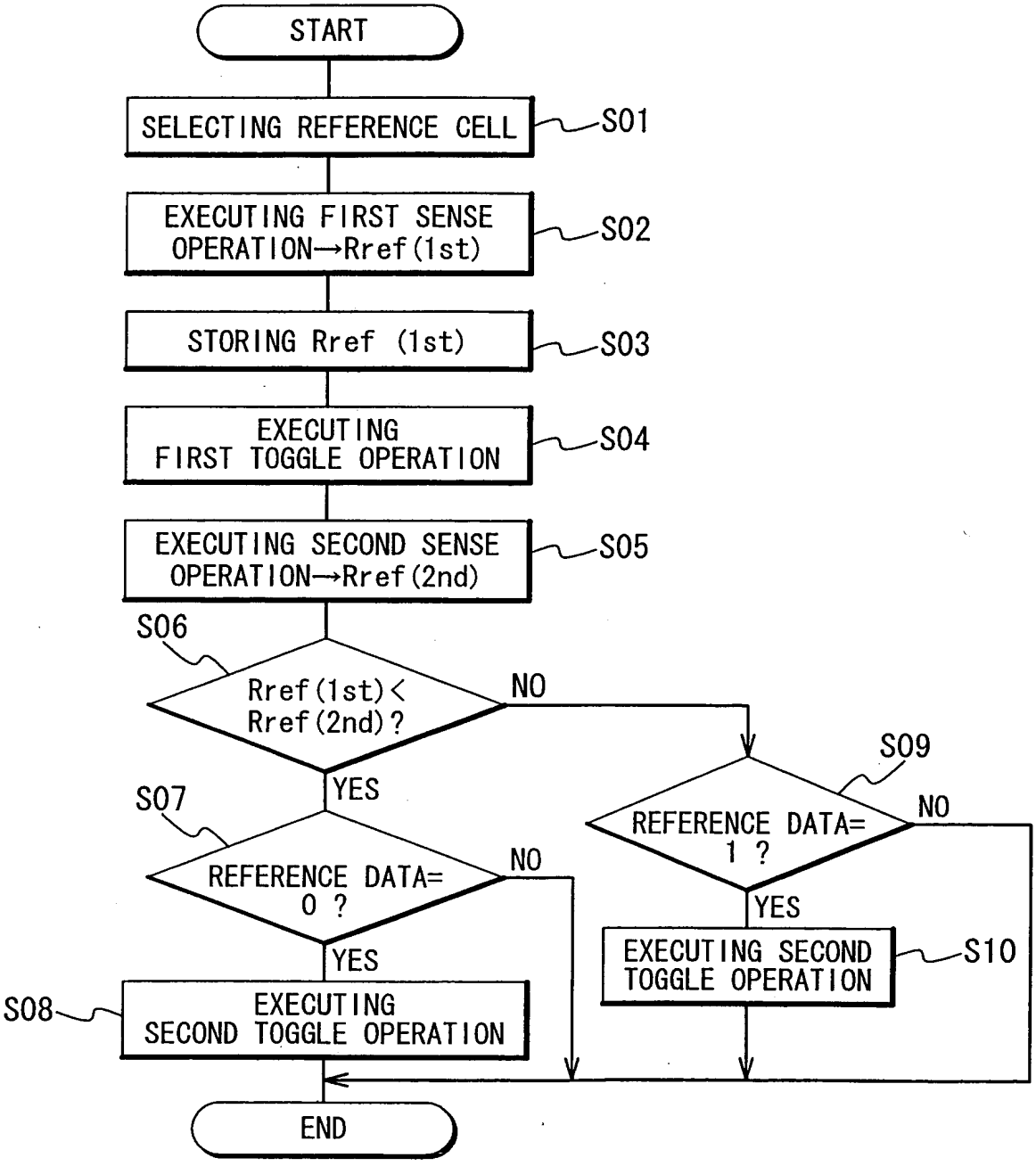

START
SELECTING REFERENCE CELL
S01
EXECUTING FIRST SENSE OPERATION→Rref(1st)
S02
STORING Rref (1st)
S03
EXECUTING FIRST TOGGLE OPERATION
S04
EXECUTING SECOND SENSE OPERATION→Rref(2nd)
S05
S06
Rref(1st)< Rref(2nd)?
NO
YES
S07
REFERENCE DATA= 0 ?
NO
YES
S08
EXECUTING SECOND TOGGLE OPERATION
S09
REFERENCE DATA= 1 ?
NO
YES
EXECUTING SECOND TOGGLE OPERATION
S10
END

Fig. 10

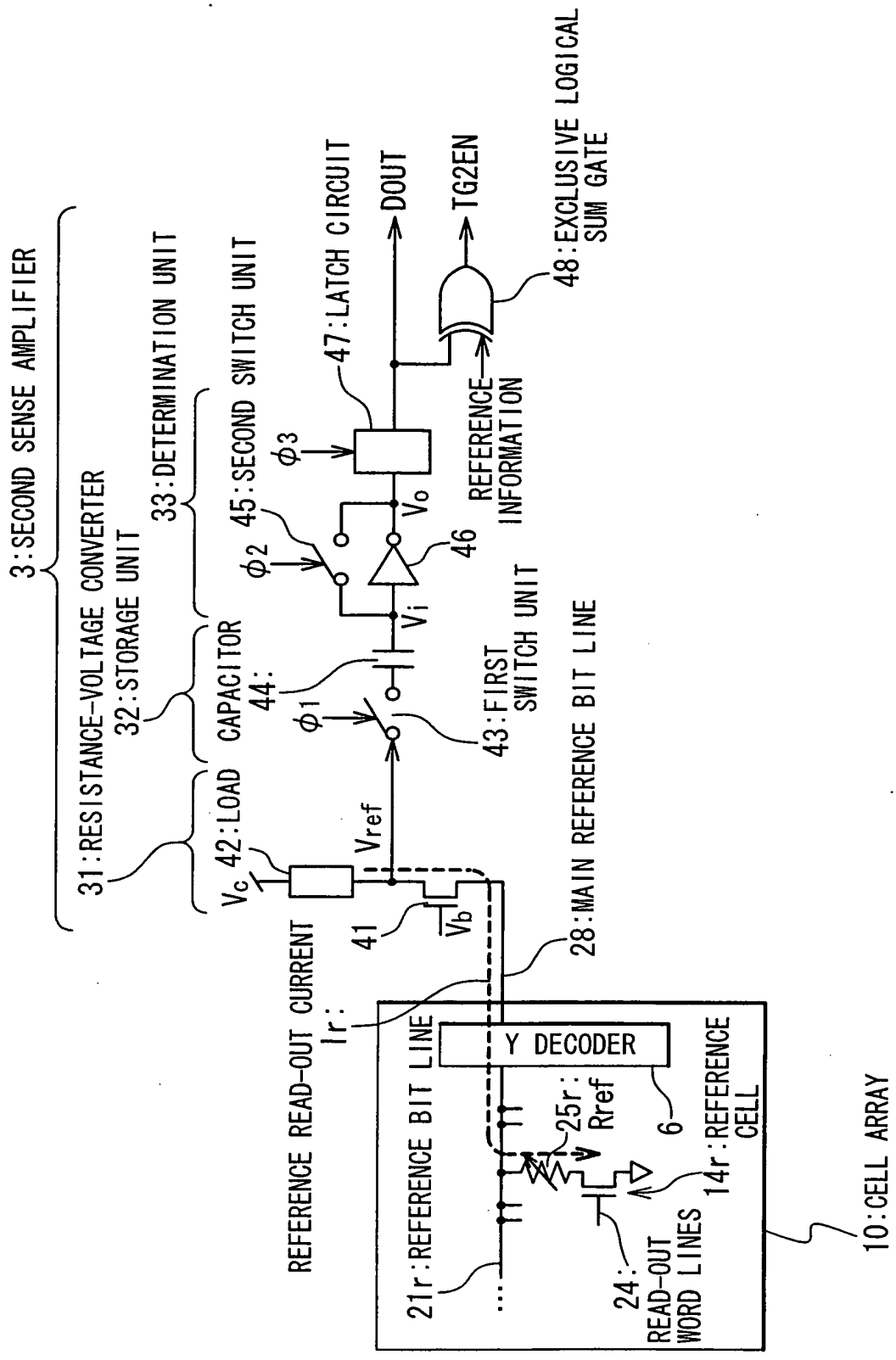

3:SECOND SENSE AMPLIFIER
31:RESISTANCE-VOLTAGE CONVERTER
32:STORAGE UNIT
33:DETERMINATION UNIT
42:LOAD CAPACITOR
44:
45:SECOND SWITCH UNIT
47:LATCH CIRCUIT
DOUT
TG2EN
48:EXCLUSIVE LOGICAL SUM GATE
REFERENCE INFORMATION
46
43:FIRST SWITCH UNIT
28:MAIN REFERENCE BIT LINE
REFERENCE READ-OUT CURRENT
Ir:
41
Y DECODER
6
21r:REFERENCE BIT LINE
25r:
Rref
14r:REFERENCE CELL
24:
READ-OUT WORD LINES
10:CELL ARRAY

Fig. 11

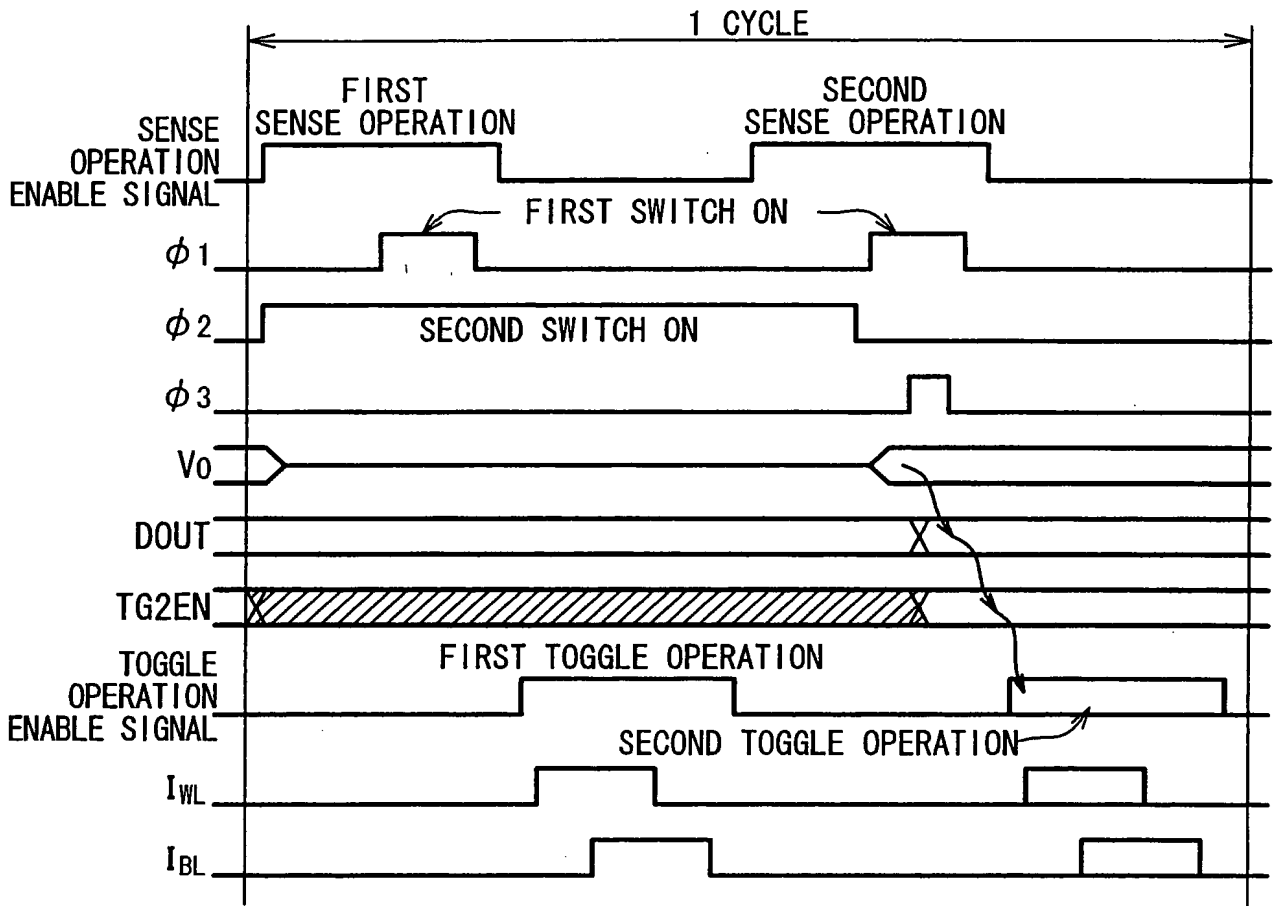

1 CYCLE
FIRST SENSE OPERATION
SECOND SENSE OPERATION
SENSE OPERATION ENABLE SIGNAL
FIRST SWITCH ON
φ1
φ2
SECOND SWITCH ON
φ3
Vo
DOUT
TG2EN
FIRST TOGGLE OPERATION
TOGGLE OPERATION ENABLE SIGNAL
SECOND TOGGLE OPERATION
I_{WL}
I_{BL}

Fig. 12

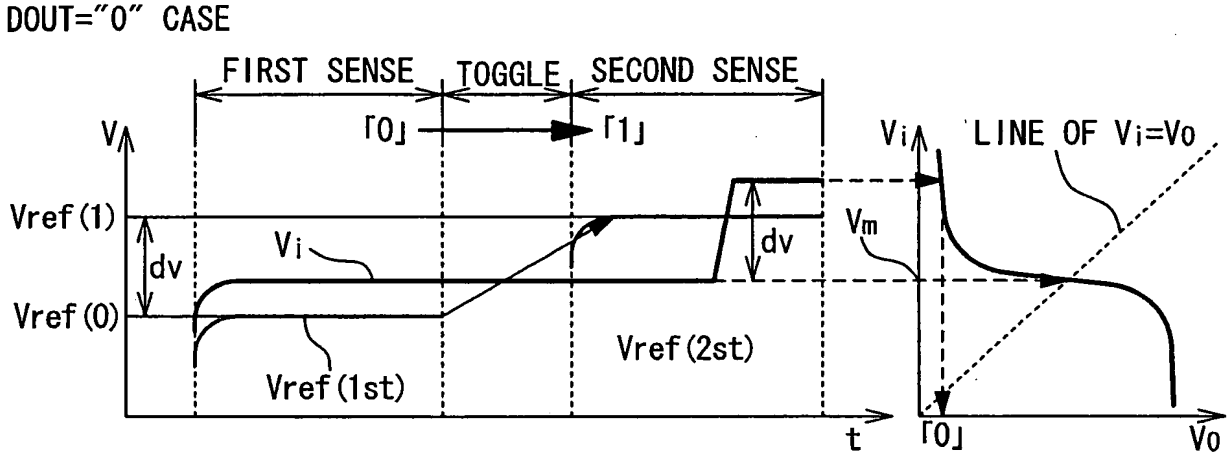

DOUT="0" CASE
FIRST SENSE
TOGGLE
SECOND SENSE
V
「0」
「1」
Vref(1)
dv
Vi
Vref(0)
Vref(1st)
Vref(2st)
dv
t
Vi
LINE OF Vi=Vo
Vm
「0」
Vo

Fig. 13

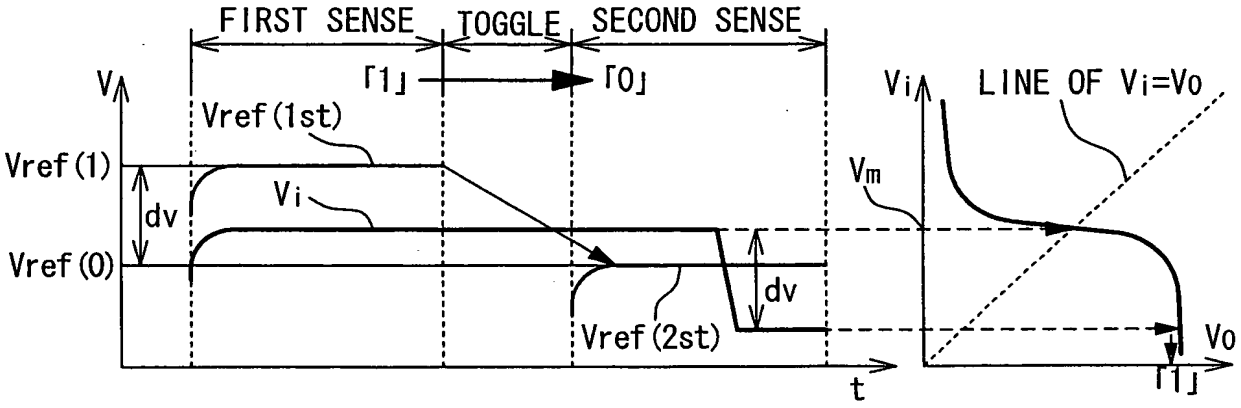

DOUT="1" CASE
FIRST SENSE
TOGGLE
SECOND SENSE
V
「1」
「0」
Vref(1st)
Vref(1)
dv
Vi
Vref(0)
dv
Vref(2st)
t
Vi
LINE OF Vi=Vo
Vm
Vo
「1」

Fig. 14

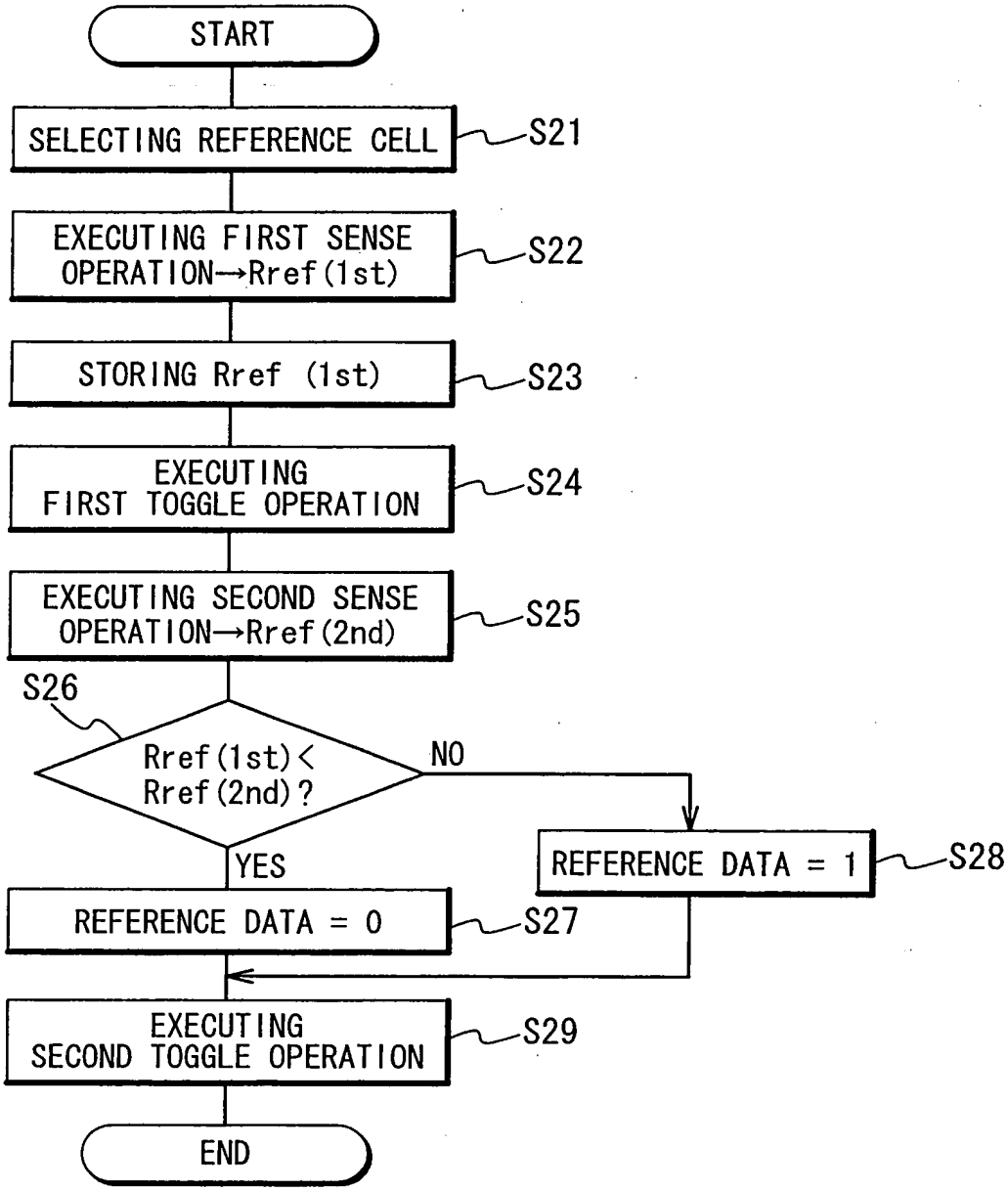

START
SELECTING REFERENCE CELL
S21
EXECUTING FIRST SENSE OPERATION→Rref(1st)
S22
STORING Rref (1st)
S23
EXECUTING FIRST TOGGLE OPERATION
S24
EXECUTING SECOND SENSE OPERATION→Rref(2nd)
S25
S26
Rref(1st)< Rref(2nd)?
NO
YES
REFERENCE DATA = 1
S28
REFERENCE DATA = 0
S27
EXECUTING SECOND TOGGLE OPERATION
S29
END

Fig. 15

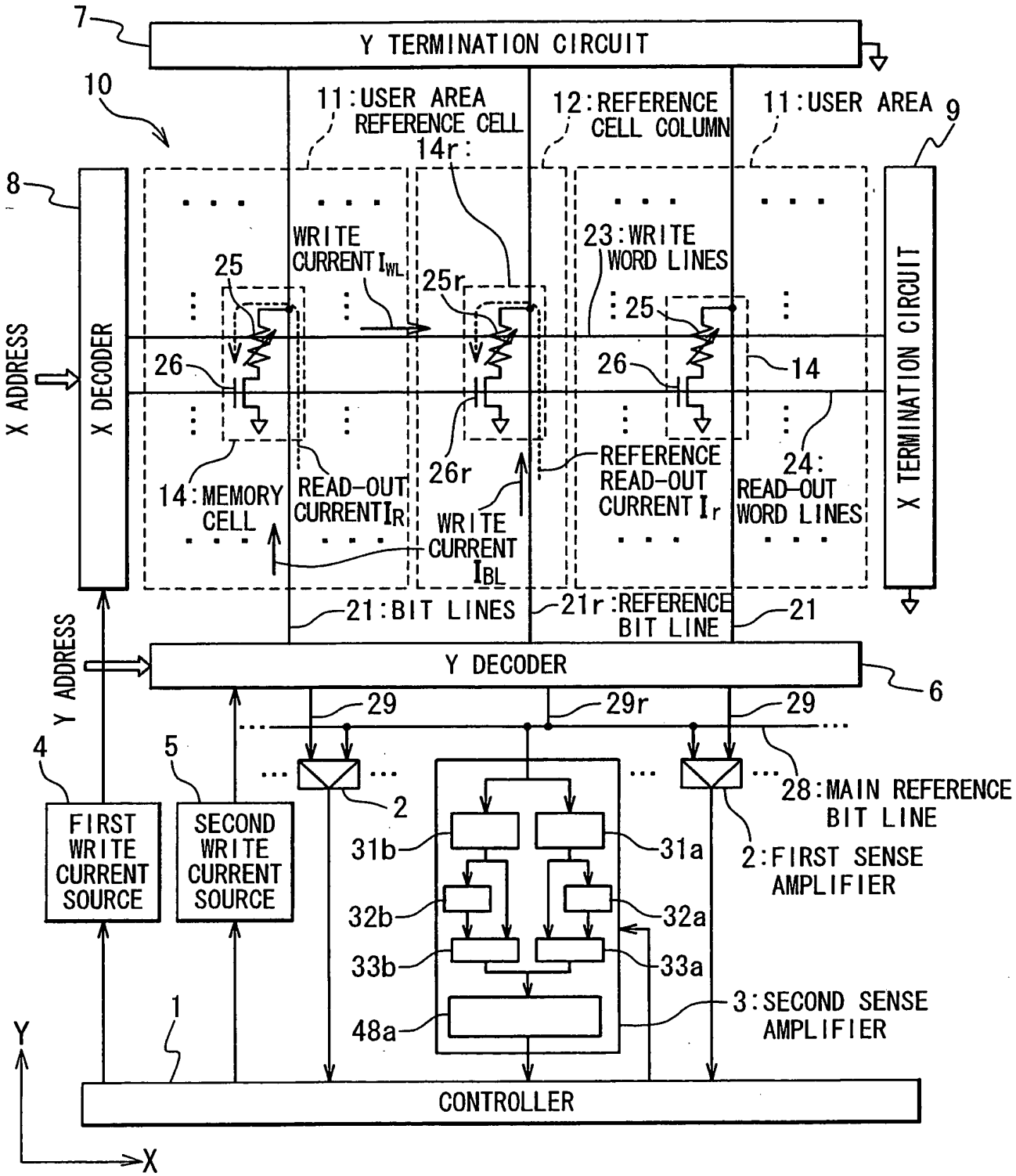

7
Y TERMINATION CIRCUIT
10
11:USER AREA
REFERENCE CELL
14r:
12:REFERENCE
CELL COLUMN
11:USER AREA
9
8
X ADDRESS
X DECODER
WRITE
CURRENT I_{WL}
25
25r
23:WRITE
WORD LINES
25
26
26
14
X TERMINATION CIRCUIT
14:MEMORY
CELL
READ-OUT
CURRENT I_R
26r
WRITE
CURRENT
I_{BL}
REFERENCE
READ-OUT
CURRENT I_r
24:
READ-OUT
WORD LINES
21:BIT LINES
21r:REFERENCE
BIT LINE
21
Y ADDRESS
Y DECODER
6
29
29r
29
4
5
2
28:MAIN REFERENCE
BIT LINE
FIRST
WRITE
CURRENT
SOURCE
SECOND
WRITE
CURRENT
SOURCE
31b
31a
2:FIRST SENSE
AMPLIFIER
32b
32a
33b
33a
3:SECOND SENSE
AMPLIFIER
48a
1
Y
X
CONTROLLER

Fig. 16

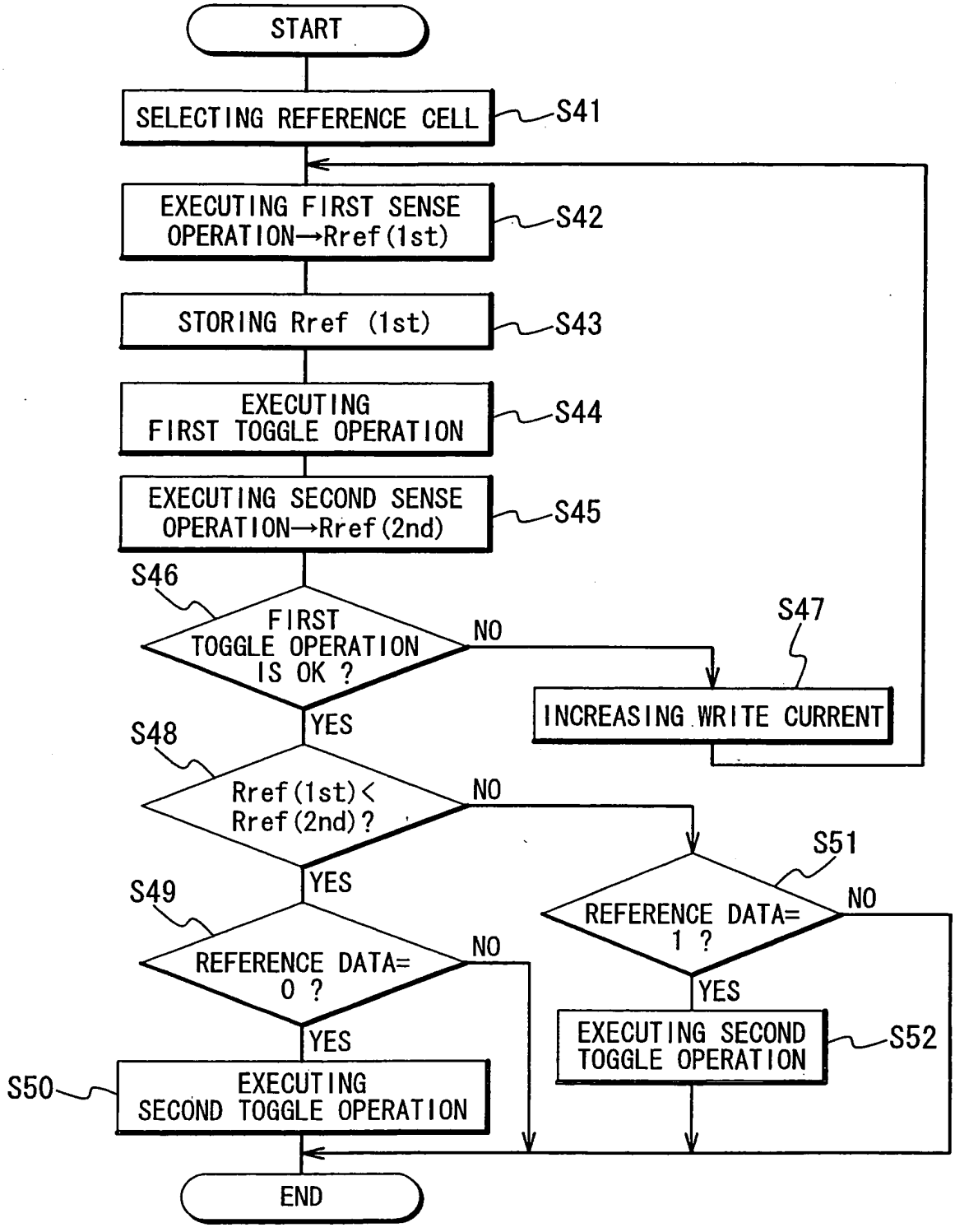

START
SELECTING REFERENCE CELL
S41
EXECUTING FIRST SENSE OPERATION→Rref(1st)
S42
STORING Rref (1st)
S43
EXECUTING FIRST TOGGLE OPERATION
S44
EXECUTING SECOND SENSE OPERATION→Rref(2nd)
S45
S46
FIRST TOGGLE OPERATION IS OK ?
NO
S47
INCREASING WRITE CURRENT
YES
S48
Rref(1st)< Rref(2nd)?
NO
YES
S49
REFERENCE DATA= 0 ?
NO
YES
S50
EXECUTING SECOND TOGGLE OPERATION
S51
REFERENCE DATA= 1 ?
NO
YES
EXECUTING SECOND TOGGLE OPERATION
S52
END

Fig. 17

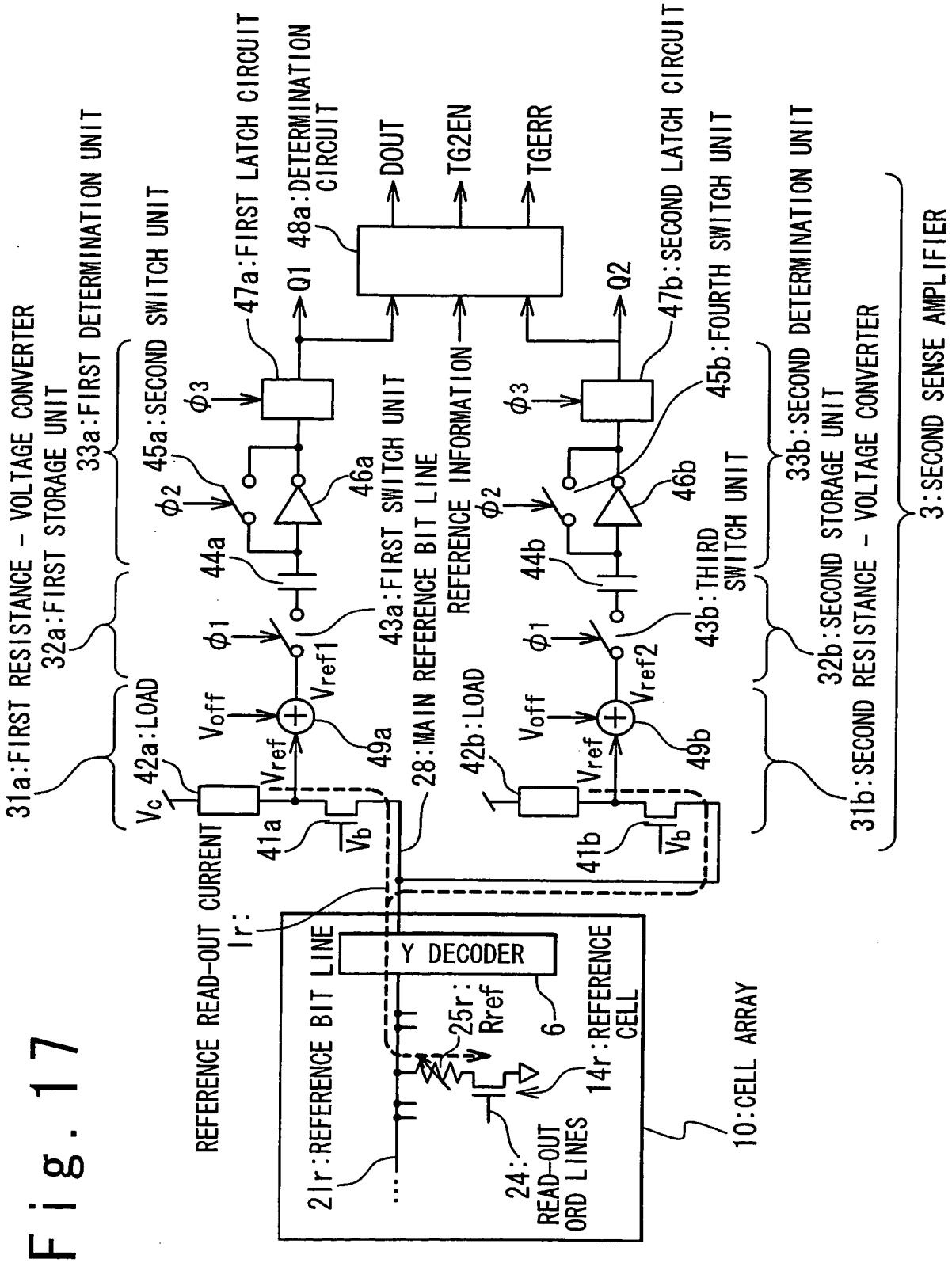

3:SECOND SENSE AMPLIFIER
31a:FIRST RESISTANCE - VOLTAGE CONVERTER
32a:FIRST STORAGE UNIT
33a:FIRST DETERMINATION UNIT
31b:SECOND RESISTANCE - VOLTAGE CONVERTER
32b:SECOND STORAGE UNIT
33b:SECOND DETERMINATION UNIT
42a:LOAD
42b:LOAD
45a:SECOND SWITCH UNIT
45b:FOURTH SWITCH UNIT
47a:FIRST LATCH CIRCUIT
47b:SECOND LATCH CIRCUIT
48a:DETERMINATION CIRCUIT
DOUT
TG2EN
TGERR
Q1
Q2
43a:FIRST SWITCH UNIT
43b:THIRD SWITCH UNIT
REFERENCE INFORMATION
28:MAIN REFERENCE BIT LINE
REFERENCE READ-OUT CURRENT
Ir:
Y DECODER
6
25r:
Rref
14r:REFERENCE CELL
21r:REFERENCE BIT LINE
24:
READ-OUT
ORD LINES
10:CELL ARRAY
Vc
Voff
Vref
Vref1
Vref2
Vb
φ1
φ2
φ3
41a
41b
44a
44b
46a
46b
49a
49b

Fig. 18

ID	REFERENCE INFORMATION	Q1	Q2	DOUT	TG2EN	TGERR
1	0	0	0	0	1	0
2	0	0	1	X	0	1
3	0	1	0	X	0	1
4	0	1	1	1	0	0
5	1	0	0	0	0	0
6	1	0	1	X	0	1
7	1	1	0	X	0	1
8	1	1	1	1	1	0

Fig. 19

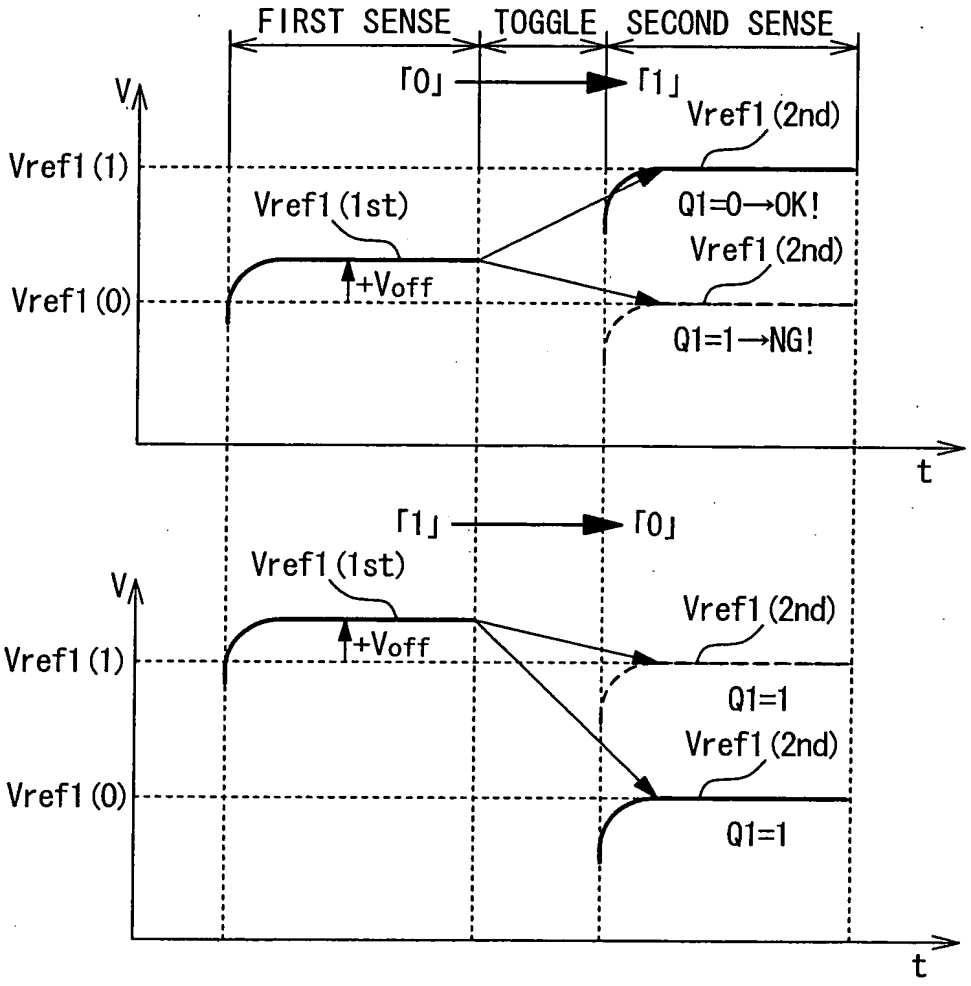

FIRST SENSE
TOGGLE
SECOND SENSE
「0」
「1」
V
Vref1 (2nd)
Vref1 (1)
Vref1 (1st)
Q1=0→OK!
Vref1 (2nd)
+Voff
Vref1 (0)
Q1=1→NG!
t
「1」
「0」
Vref1 (1st)
V
Vref1 (2nd)
+Voff
Vref1 (1)
Q1=1
Vref1 (2nd)
Vref1 (0)
Q1=1
t

Fig. 20

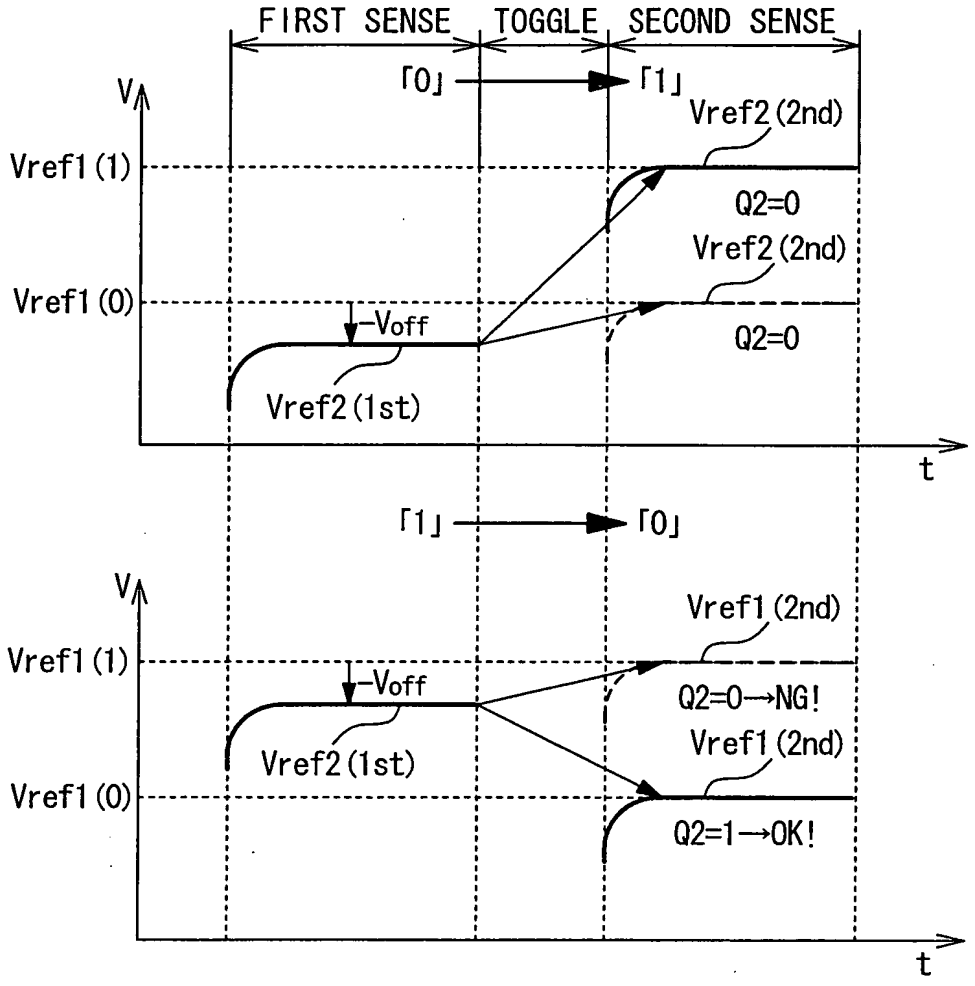
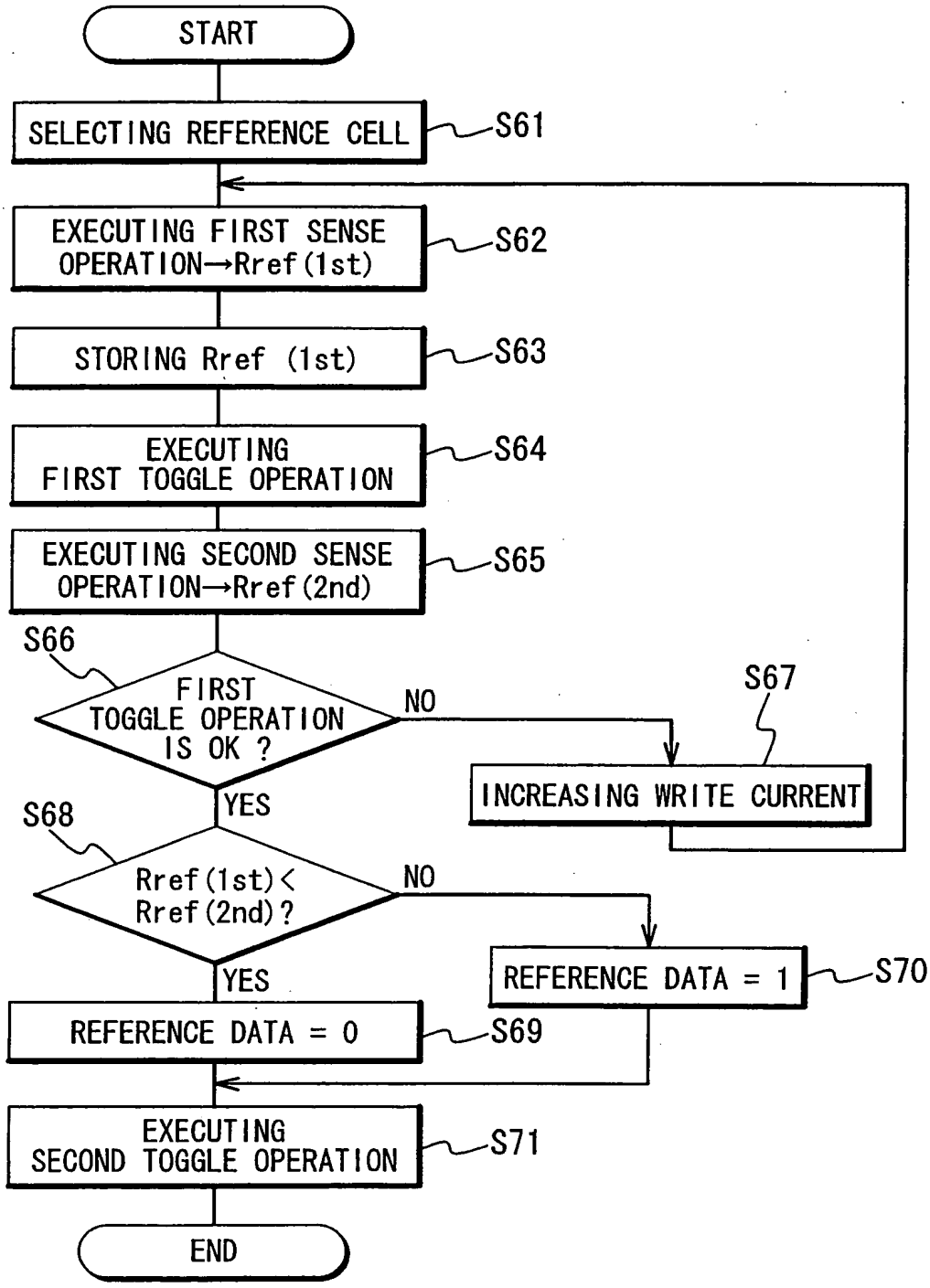

FIRST SENSE
TOGGLE
SECOND SENSE
「0」
「1」
V
Vref1 (1)
Vref2 (2nd)
Q2=0
Vref2 (2nd)
Vref1 (0)
-Voff
Q2=0
Vref2 (1st)
t
「1」
「0」
V
Vref1 (2nd)
Vref1 (1)
-Voff
Q2=0→NG!
Vref1 (2nd)
Vref2 (1st)
Vref1 (0)
Q2=1→OK!
t

Fig. 21


START
SELECTING REFERENCE CELL
S61
EXECUTING FIRST SENSE OPERATION→Rref(1st)
S62
STORING Rref (1st)
S63
EXECUTING FIRST TOGGLE OPERATION
S64
EXECUTING SECOND SENSE OPERATION→Rref(2nd)
S65
S66
FIRST TOGGLE OPERATION IS OK ?
NO
S67
INCREASING WRITE CURRENT
YES
S68
Rref(1st)< Rref(2nd)?
NO
REFERENCE DATA = 1
S70
YES
REFERENCE DATA = 0
S69
EXECUTING SECOND TOGGLE OPERATION
S71
END